Instrução Resto (MOD)

Especificado por: Fluxo geral, fluxo detalhado e máquina de estado em Verilog.

1. Fluxo Geral

MAH <- M[PC]

PC <- PC + 1

MAL <- M[PC]

PC <- PC + 1

MD <- M[MA]

AC <- MD

M[SP] <- RFLAGS

SP <- SP - 1

Push

Accumulator

M[SP] <- AC

SP <- SP - 1

MD <- AC

AC <- AC + MD

MD <- MDL

AC <- SHR(AC)

AC <- SHR(AC)

MD <- AC

SP <- SP + 1

AC <- M[SP]

SP <- SP + 1

RFLAGS <- M[SP]

Pop Accumulator

AC <- MDH

AC <- SHR(AC)

AC <- SHR(AC)

MD < 1

ERROR

AC <- AC - MD

AC < MD

0 1

OBS.: MOD2 e MOD3 são apenas “labels”.

1. Fluxo Detalhado

T4

ENPCA

T5

ENPCA

MR

ENPCA

MR

(LMAH)

T6

T7

(INCPC)

T8

ENPCA

ENPCA

MR

(LMAL)

ENPCA

MR

T9

T10

T11

(INCPC)

ENMAA

ENMAA

MR

T12

T13

ENMAA

MR

(LMD)

ENDES

(LAC)

T14

T15

ENSPA

ENFLD

ENSPA

ENFLD

MW

T16

(DECSP)

T17

ENSPA

ENDES

T18

ENSPA

ENDES

MW

T19

(DECSP)

(LRESET)

(LINT)

T20

ENDES

(LMD)

T21

T22

ENDES

OP2

(LAC)

(LRESET)

(LINT)

ENDES

(LMD)

ENDES

OP2

(LAC)

(LRESET)

(LINT)

T23

T24

ENDES

(LMD)

ENDES

OP2

(LAC)

(LRESET)

(LINT)

ENDES

(LMD)

ENDES

OP2

(LAC)

(LRESET)

(LINT)

T25

T26

T27

T28

T29

ENDES

SD0

(LAC)

(LRESET)

(LINT)

ENDES

SD0

(LAC)

(LRESET)

(LINT)

T30

ENDES

SD0

(LAC)

(LRESET)

(LINT)

T31

ENDES

SD0

(LAC)

(LRESET)

(LINT)

T32

ENDES

(LMD)

T33

(INCSP)

T34

T35

ENSPA

ENSPA

MR

(LAC)

ENSPA

MR

T36

T37

ENSPA

MR

ENSPA

(INCSP)

T38

T39

T40

T41

ENSPA

MR

(LINTE)

(LCARRY)

(LZERO)

(LRESET)

(LINT)

ENDES

SD0

(LAC)

(LRESET)

(LINT)

ENDES

SD0

(LAC)

(LRESET)

(LINT)

T42

T43

T44

ENDES

SD0

(LAC)

(LRESET)

(LINT)

T45

ENDES

SD0

(LAC)

(LRESET)

(LINT)

MD < 1

ERROR

T0

AC < MD

TN

ENDES

OP2

OP1

(LAC)

SCZ

(LCARRY)

(LRESET)

(LINT)

T45

T0

1. Máquina de Estados

module mod(T1, clock);

reg [32: begin0] T;

input clock;

output SIGNAL;

always @(negedge clock) begin

ENPCA = 0;

MR = 1;

LMAH = 0;

LMAL = 0;

INCPC = 0;

ENMAA = 0;

LMD = 0;

DECSP = 0;

ENDES = 0;

LAC = 0;

LMD = 0;

LAAC = 0;

LINT = 0;

LINTE = 0;

LRESET = 0;

SD0 = 0;

OP1 = 0;

OP2 = 0;

ENSPA = 0;

ERROR = 0;

end

always @(posedge clock) //begin

case (T) //begin

4: begin

ENPCA = 1;

T = 5;

end

5: begin

ENPCA = 1;

MR = 0;

T = 6;

end

6: begin

ENPCA = 1;

MR = 0;

LMAH = 1;

T = 7;

end

7: begin

INCPC = 1;

T = 8;

end

8: begin

ENPCA = 1;

T = 9;

end

9: begin

ENPCA = 1;

MR = 0;

T = 10;

end

10: begin

ENPCA = 1;

MR = 0;

LMAL = 1;

T = 11;

end

11: begin

INCPC = 1;

ENMAA = 1;

T = 12;

end

12: begin

ENMAA = 1;

MR = 0;

T = 13;

end

13: begin

ENMAA = 1;

MR = 0;

LMD = 1;

T = 14;

end

14: begin

ENDES = 1;

LAC = 1;

T = 15;

end

15: begin

ENSPA = 1;

ENFLD = 1;

T = 16;

end

16: begin

ENSPA = 1;

ENFLD = 1;

MW = 0;

T = 17;

end

17: begin

DECSP = 1;

T = 18;

end

18: begin

ENSPA = 1;

ENDES = 1;

T = 19;

end

19: begin

ENSPA = 1;

ENDES = 1;

MW = 0;

T = 20;

end

20: begin

DECSP = 1;

LRESET = 1;

LINT = 1;

T = 21;

end

21: begin

ENDES = 1;

LMD = 1;

T = 22;

end

22: begin

ENDES = 1;

OP2 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 25;

end

23: begin

ENDES = 1;

LMD = 1;

T = 24;

end

24: begin

ENDES = 1;

OP2 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 25;

end

25: begin

ENDES = 1;

LMD = 1;

T = 26;

end

26: begin

ENDES = 1;

OP2 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 27;

end

27: begin

ENDES = 1;

LMD = 1;

T = 28;

end

28: begin

ENDES = 1;

OP2 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 29;

end

29: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 30;

end

30: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 31;

end

31: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 32;

end

32: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 33;

end

33: begin

ENDES = 1;

LMD = 1;

T = 34;

end

34: begin

INCSP = 1;

T = 35;

end

35: begin

ENSPA = 1;

T = 36;

end

36: begin

ENSPA = 1;

MR = 0;

T = 37;

end

37: begin

ENSPA = 1;

MR = 0;

LAC = 1;

T = 38;

end

38: begin

INCSP = 1;

T = 39;

end

39: begin

ENSPA = 1;

T = 40;

end

40: begin

ENSPA = 1;

MR = 0;

T = 41;

end

41: begin

ENSPA = 1;

MR = 0;

LINTE = 1;

LCARRY = 1;

LZERO = 1;

LRESET = 1;

LINT = 1;

T = 42;

end

42: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 43;

end

43: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 44;

end

44: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

T = 45;

end

45: begin

ENDES = 1;

SD0 = 1;

LAC = 1;

LRESET = 1;

LINT = 1;

if(MD < 1) begin

ERROR=1;

T = 0;

end else begin

T = 46;

end

end

46: begin

ENDES = 1;

LACC = 1;

if(AC<MD) begin

ENDES = 1;

OP2 = 1;

OP1 = 1;

LAC = 1;

SCZ = 1;

LCARRY = 1;

LRESET = 1;

LINT = 1;

T = 45;

end else begin

T = 0;

end

end

default: begin

T=0;

end

endcase

//end

endmodule